HIGHLY PRODUCIBLE MONOLITHIC Q-BAND MESFET VCO

Scott Martin, Shirley Meyer, Eli Reese, and Keith Salzman

Texas Instruments Incorporated
Dallas, Texas 75265

ABSTRACT

A fully monolithic self-biased VCO has been demonstrated at 40 GHz. A buffer amplifier, all bias elements, and a tuning varactor have been integrated on a 4.4- × 2.0-mm chip. Gate lengths of 0.35 μm were used in for this FET based oscillator that delivers greater than 90 mW of output power over a tuning bandwidth of 2.8 Ghz.

INTRODUCTION

Improvements in GaAs material and device processing have extended the operation range of the GaAs MESFET well into Q-band. Fundamental mode MESFET oscillators have shown output powers at lower millimeter-wave frequencies that approach the level of performance of Gunn diodes[1,2]. MESFET oscillators have an advantage over Gunn diodes because of the efficiency and level of integration that are achievable. GaAs monolithic VCOs have been developed at Ka-band that integrate vertical varactors with the planar structure of the MESFET[2]. These authors have reported an output power of 60 mW for a VCO with a 1-percent tuning bandwidth (300 MHz) centered at 31 GHz. This work was accomplished by integrating a high Q vertical varactor with a high F_t planar MESFET on a multilayered epitaxial substrate. Inherent in this approach is an increase in process complexity. More recent transmitters have been reported that deliver as much as 140 mW over a 2-percent tuning bandwidth (600 MHz) centered at 35 GHz[3,4]. Frequency agility was implemented by varying V_{gs} on the oscillator FET. The disadvantage of this approach is limited tuning bandwidth and performance degradation as device pinch off is approached. One author[4] reports a 40-percent RF yield for an output power and tuning range specification of 17 dBm and 400 MHz respectively. A frequency distribution histogram for the transmitter in reference [4] also shows a standard deviation of approximately 300 MHz for a transmitter with a total tuning range of 600 MHz.

This paper describes a highly integrated fully monolithic Q-band VCO that is built on a uniformly doped epitaxially grown substrate using 0.35 μm gates. This FET based oscillator delivers greater than 90 mW of output power at a frequency of 40 GHz with 2.8 GHz of tuning bandwidth. Tuning is achieved via an integrated varactor. A four stage buffer amplifier and all bias networks have been included on chip to minimize performance variation due to assembly tolerances and load variations.

DESIGN OBJECTIVES

The objective of this effort was to produce a cost effective millimeter-wave oscillator for a high volume application. Attention to overall device and assembly yields was necessary to minimize the RF yielded cost per mm^2. Device yields were to be maximized by using 0.35-μm length gates on a uniformly doped GaAs MBE grown substrate. Assembly yields were to be maximized by increasing the level of integration of the monolithic, providing for thin wafer RF probe capability, and making the die compatible with automated assembly requirements.

Typical VCO applications require some element to provide isolation of the oscillator from load variations. This can be accomplished by the use of a buffer amplifier or a ferrite based component. The interconnect to this isolation element can cause performance variations. Also, the impedance of bonding wires at millimeter-wave frequencies can be difficult to absorb into the matching networks of the isolation elements. It was determined that the best approach to minimize the performance variations due to load uncertainties and assembly tolerances was to integrate a buffer amplifier on the oscillator chip. The buffer amplifier can also be used to flatten the output power and present the oscillator with an optimum terminating impedance.

DESIGN

The oscillator is a 210-μm device with six 35-μm width fingers in a common gate configuration with the output taken from the drain. The varactor is placed in a resonant structure on the gate side. The varactor was designed to have a capacitance ratio of approximately 3:1 and a starting value of 0.2 pF. The buffer amplifier is a

92CH3162-5/92/0000-0057$01.00 © 1992 IEEE

four stage single ended design with a total periphery of 1050 μm. All FETs are self-biased which allows device operation from a single polarity power supply. A photograph of the chip is given in Figure 1 and the electrical schematic is shown in Figure 2. The chip has overall dimensions of 4.4 × 2.0 mm and has a ground-signal RF probe pad for compatibility with thin wafer RF probing.

FABRICATION

The material used for fabrication was MBE grown GaAs on a semi-insulating GaAs substrate. First, a 100,000 Å unintentionally doped buffer layer was grown, with measured carrier concentration typically 10^{14} to 10^{15} cm^{-3}. On the buffer is a 1500 Å Si-doped active layer with a nominal carrier concentration of 4.5×10^{17} cm^{-3}. A 1000 Å Si-doped layer with a carrier concentration of 2-3 $\times 10^{18}$ cm^{-3} is used to provide improved ohmic contact for the devices.

MESFETs and the varactor for the MMIC were fabricated using Au/Ge alloy for ohmic contacts and boron implantation for device isolation. A dual recess configuration was used for the gate channels to reduce the detrimental effects of the contact layer near the gate. E-beam lithography was used to pattern wide and narrow recesses for the devices and Ti/Pt/Au gates self-aligned in the narrow recess. A H_2O_2/H_2SO_4-based etch was used in recessing the devices to a target current for both recesses.

The gate length for the device is desired to be as short as possible for high frequency performance, but fabricated using procedures as close as possible to those used for standard ½-μm devices. To balance the gate length decrease versus an increase in gate resistance, the resist layer used for e-beam lithography and the titanium layer were reduced in thickness to provide reproducible and reliable gates. The necessary parameters were optimized to produce nominally 0.35-μm gates with 500 Ω/mm of gate metal resistance.

Plated transmission line barriers and capacitor bottom plates were defined using metal evaporations including titanium as a diffusion barrier and chromium as an etch stop for backside vias. A 2000 Å layer is used for both the capacitor dielectric and FET passivation. Transmission lines and interconnect airbridges are then patterned and electroplated with gold. Following completion of the front side, a DC probe is done to screen nonfunctional devices.

For the backside, wafers were lapped to 100 μm and vias for backside connections were patterned and etched using a Freon 12 based RIE process. Finally, the

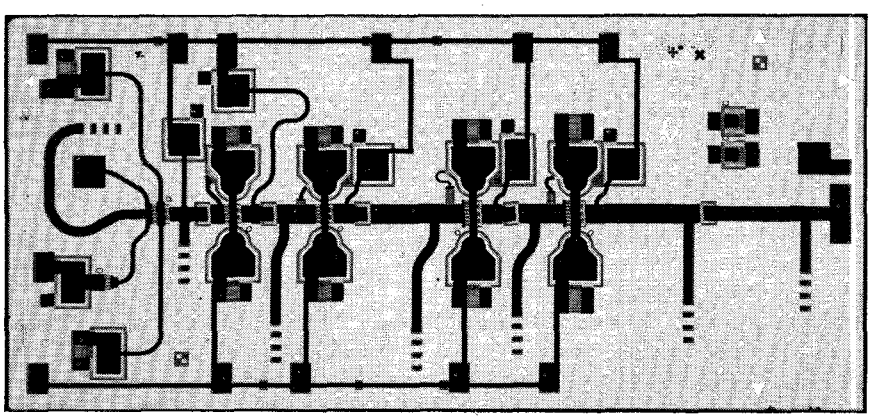

Figure 1. Photograph of the Q-Band VCO

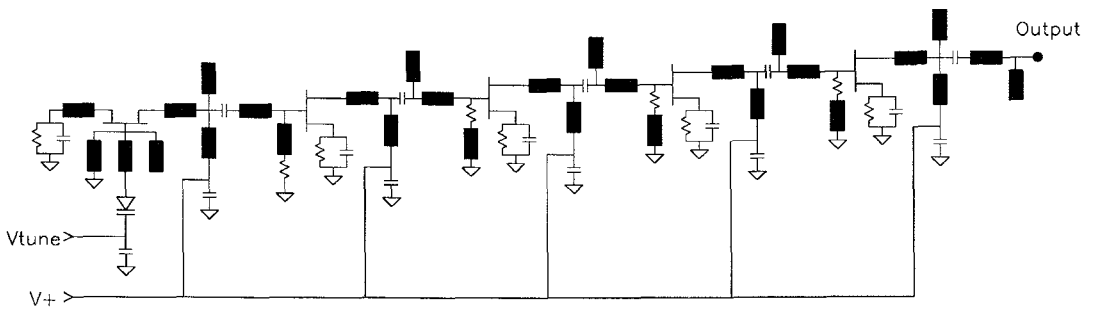

Figure 2. Schematic of the Q-Band VCO

backside ground plane was gold plated and the wafers scribed to separate individual die.

OSCILLATOR PERFORMANCE

Figure 3 is the frequency response for a typical VCO when biased at 6.5 volts and 245 mA. For a tuning voltage of 0 to 8.0 volts, a tuning bandwidth of 2.8 GHz was achieved. The modulation sensitivity has less than a 3:1 variation across the given bandwidth. The uncorrected temperature coefficient is approximately -4.5 MHz/°C. Also included in Figure 3 is the measured output power. The room temperature output power is approximately 19.75 dBm with a variation of less than ±0.4 dB over the 2.8 GHz tuning range. The temperature coefficient for the output power is approximately -0.015 dB/°C. Frequency pulling into a 1.7:1 load is less than 30MHz. Frequency pushing is less than 50 MHz/V.

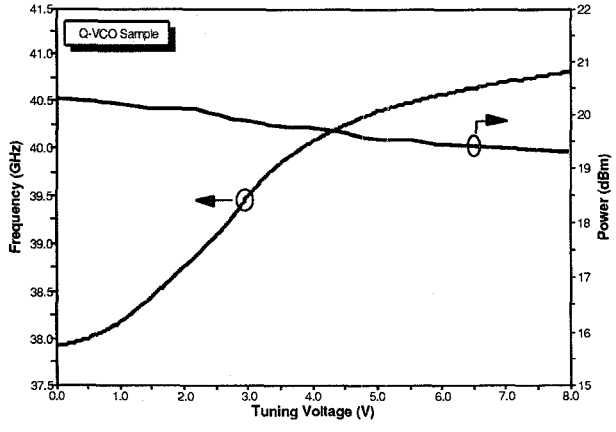

Figure 3. Frequency and Output Power as a Function of Tuning Voltage for a Typical Q-VCO

To demonstrate the producibility of this design, two lots of four wafers each were processed with this design. These eight wafers had a final DC yield of approximately 70 percent when measured against standard Texas Instruments DC autoprobe limits. Fixtured RF data was measured on 100 randomly selected DC yielded devices. The population was evenly distributed across four wafers from one lot. The RF yield for a minimum power of 17.5 dBm and a tuning bandwidth of 1.5 GHz was 100 percent.

The statistical information from this 100 sample database is given in Figures 4 through 8. Note that the output power and frequency distributions are tightly grouped for these devices. The mean output power in Figure 4 is approximately 19.7 dBm with a flatness of better than 0.25 dB over a 1 GHz bandwidth. Figures 5, 6, 7, and 8 are histograms of the frequency, modulation sensitivity, modulation sensitivity deviation, and output power distribution for a fixed tuning voltage.

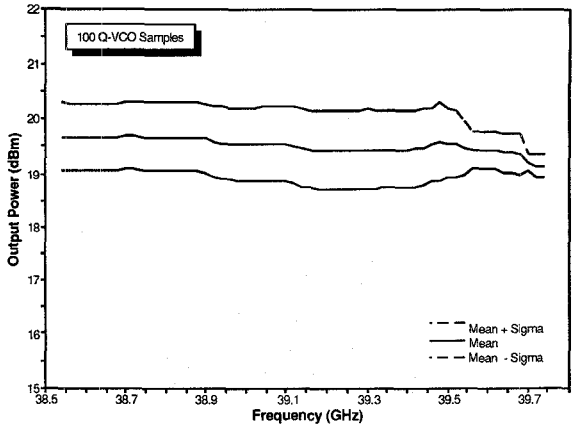

Figure 4. Output Power as a Function of Frequency for 100 Q-VCO Samples

The histogram in Figure 5 shows the distribution of operating frequencies for the 100 samples at a constant tuning voltage. The frequency of operation of an oscillator is very sensitive to the reactive circuit elements. Typically, the most sensitive reactive elements are those associated with the FETs and varactors whose values will vary within the limits of process control. The distribution of the frequency of oscillation for a fixed tuning voltage is a good gauge of FET and varactor process variation from one device to another. The standard deviation is approximately 200 MHz and is a small percentage of the operating frequency (0.5 percent) and the total tuning range (8 percent) showing good uniformity from device-to-device and wafer-to-wafer.

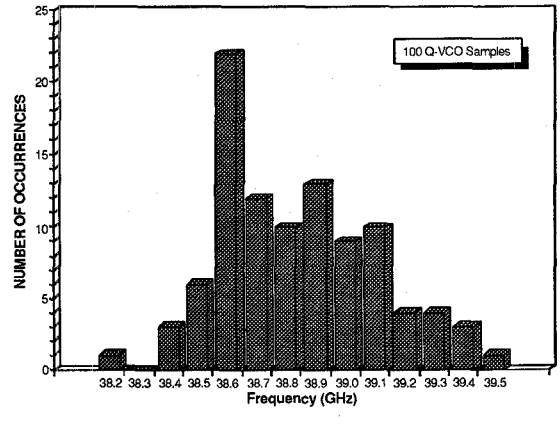

Figure 5. Frequency Distribution for a Fixed Tuning Voltage

The modulation sensitivity distribution at a fixed tuning voltage is given in Figure 6. The mean value is approximately 500 MHz/V and the standard deviation is less than 100 MHz/V. The distribution of the modulation sensitivity deviation from a nominal value is shown in Figure 7 expressed as a percentage. These worst case deviations are calculated for a tuning range of 100 MHz.

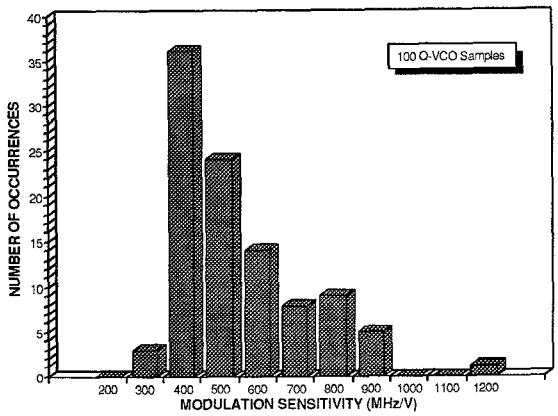

Figure 6. Modulation Sensitivity Distribution for a Fixed Tuning Voltage

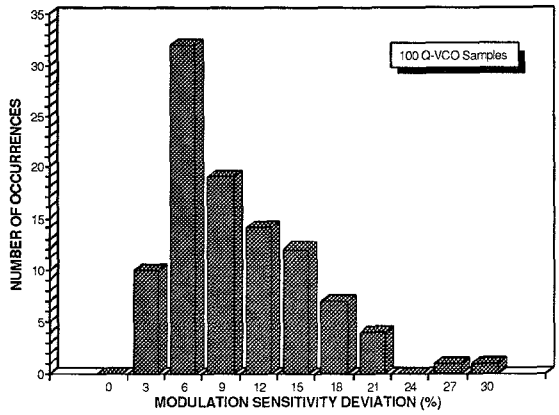

Figure 7. Modulation Sensitivity Deviation in a 100-MHz Tuning Bandwidth

The tuning voltage at the center of the 100-MHz tuning range is common to all samples. The mean deviation error is approximately 9 percent and the standard deviation is 3 percent. The output power distribution is given in Figure 8. The mean value is 19.6 dBm and the standard deviation is approximately 0.4 dB.

CONCLUSION

A fully monolithic self-biased VCO with an integrated varactor and buffer amplifier has been demonstrated at 40 GHz. This performance was achieved using gates of 0.35 μm length on a uniformly doped MBE substrate. The output power for 100 samples taken from multiple

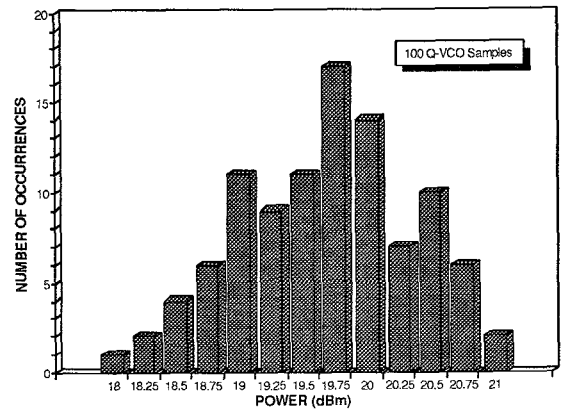

Figure 8. Output Power Distribution for a Fixed Tuning

wafers has a mean value of 19.6 dBm over a tuning bandwidth of 1.5 GHz. The standard deviation of the frequency at a fixed tuning voltage was a small percentage of the total tuning bandwidth which indicates good process control. The demonstrated performance and repeatability are consistent with that required for high volume millimeter-wave applications.

ACKNOWLEDGEMENTS

The authors would like to thank Jules Vaillancourt for help in device testing and La Joyce Doran for help in preparing the final manuscript.

REFERENCES

1. Goldwasser, R., et al, "Monolithic Ka-Band VCOs", IEEE 1988 Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 55-58.

2. McDermott, M. G., et al, "Integration of High-Q GaAs Varactor Diodes and .25 μm GaAs MESFET's for Multifunction Millimeter-Wave Monolithic Circuit Applications", IEEE Trans. on MTT, vol.38, no. 9, Sept. 1990, pp. 1183-1190.

3. Mondal, J., et al, "MESFET MMIC Ka-Band Transmitter performance for High Volume System Applications", GaAs IC Symposium Digest, 1991, pp. 153-156.

4. Wang, H., "A Monolithic Ka-Band Transmitter Using 0.25 μm GaAs MESFET Technology", GaAs IC Symposium Digest, 1991, pp. 157-160.